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Patent Application
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for

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TITLE: MAGNETIC TUNNEL JUNCTION MEMORY DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

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This application claims benefit of the filing date of U.S. Provisional Application
Serial No. 60/444,240 entitled "MAGNETIC TUNNEL JUNCTION MEMORY CELL
WITH PERPENDICULAR MAGNETIC ANISOTROPY IN FREE AND PINNED
LAYERS", filed February 1, 2003, the entire content of which is incorporated herein by
reference.

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FEDERALLY SPONSORED RESEARCH: Not Applicable

SEQUENCE LISTING: Not Applicable

FIELD OF THE INVENTION

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The present invention relates generally to the field of non-volatile memory
devices for use in computers and other devices. More particularly, the present invention

relates to magnetic tunnel junction memory cell with perpendicular orientation of magnetization in free and pinned layers of magnetic tunneling junction memory element that is used as an individual memory cell of non-volatile magnetic random access memory arrays.

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BACKGROUND OF THE INVENTION

The use of magnetic tunnel junction element in a memory cell of a non-volatile magnetic random access memory (MRAM) arrays is described in U.S. Patent No.

10 5,640,343. A typical MRAM device includes an array of memory cells positioned at the intersections of word lines and bit lines.

A typical memory cell may be composed of a magnetic tunnel junction (MTJ) memory element and a transistor or other non-linear element in series, and intersecting conductive lines. The memory cell is controlled by passing currents through two
15 conductive lines. The MTJ element and the transistor are vertically arranged in the intersection region of the two conductive lines in a vertical space between the two lines to minimize a total MRAM surface area. A typical MTJ memory element has a pinned (or fixed) magnetic layer, a free (or sense) magnetic layer, and an insulating tunnel barrier layer sandwiched between the ferromagnetic layers. The MTJ element exhibits a giant
20 tunneling magnetoresistance in the presence of a magnetic field. Relative orientations of magnetization in the free and pinned ferromagnetic layers determine the resistance of the MTJ memory element. Generally, the resistance of the MTJ element is "low" if the magnetic layers have a parallel magnetization orientation, and the resistance is increased considerably if the magnetization orientation is changed from parallel to anti-parallel.

25 These two combinations of magnetization orientations, parallel and anti-parallel, present logic values of "0" and "1". The orientation may be changed from parallel to anti-parallel or vice-versa by applying the proper magnetic field to the MTJ memory element. A logic value may be written to an MTJ cell by setting the magnetization orientation in the free layer. The logic value stored in the MTJ cell may be read by sensing the
30 resistance of the MTJ element.

Figs. 1A and 1B show a schematic view of the structure and function of a MTJ memory cell 20 according to prior art. The memory cell 20 includes a MTJ memory element 12 and transistor 14 connected in series by means of conductive lead 16, conductive stud 14 and contact pad 12, a bit line 16 and word line 18. The MTJ element 12 is vertically arranged at the intersection region of the bit 16 and word 18 lines. The MTJ memory element 12 is composed of a stack of an insulating tunnel barrier layer 15 sandwiched between two magnetic layers 11 and 13. Orientation of magnetization in both magnetic layers is parallel to a major plane (in-plane orientation) of the layers. One of the magnetic layers has a higher coercivity than that of the other magnetic layer. The magnetic layer 11 with the higher coercivity is normally called "a pinned layer". The other magnetic layer 13 with the low coercivity is normally called "a free layer". An antiferromagnetic pinning layer 17 anchors the magnetization orientation in the pinned layer 11 by means of an exchange coupling between the layers.

The orientation of magnetization in the free layer 13 may be changed by a relatively small external magnetic field (a bi-directional arrow). To change the orientation of magnetization in the pinned layer 11 much stronger external magnetic field needs to be applied (an unidirectional arrow). When the magnetization orientations of the free 13 and pinned 11 layers are anti-parallel, the resistance of the MTJ element 12 is high; when the magnetization orientations are parallel, the resistance is low. The relative variation of the resistance between these two states may be up to 40% by appropriate choice of MTJ element materials, barrier layer thickness and other parameters.

The MTJ memory element 12 is positioned between the transistor 14 and the current supply bit line 16. In a "write" mode, a current I_{w1} passing through the line 16 generates a magnetic field 19. The word line 18, orthogonal to the bit line 16 (i.e. in this case the word line 18 is perpendicular to a plane of the Fig.1A). A current I_{w2} flowing through the word line 18 generates a second magnetic field 21 (located in the plane of the figure).

In the "write" mode (Fig. 1A), the transistor 14 is blocked. The currents I_{w1} and I_{w2} flow through the bit line 16 and the word line 18, respectively. The MTJ element 12 is therefore subjected to two orthogonal magnetic fields 19 and 21, respectively. The field 19 is applied along a hard axis of magnetization in the free layer 13, in order to

reduce its switching field. The magnetic field 21 being applied along an easy axis of magnetization in order to generate a reversal of the magnetization of the free layer 13 and thus writes in the memory element 12. In principle, only the memory element 12 located in the intersection region of the lines 16 and 18 is subject to reversal, since each magnetic
5 field 19 or 21 taken individually is insufficient to cause reversal of the magnetization in the free magnetic layer 13.

In a "read" mode (Fig. 1B) the transistor 14 is opened and is held in a saturated condition (i.e. a sense current I_s flowing through it is at a maximum) by a positive bias on its gate. The current I_s flowing through the bit line 16 only passes through the MTJ
10 memory element 12 whose transistor 14 is opened. This current enables the resistance of the MTJ element 12 to be measured. By comparison with a resistance of a reference memory cell (not shown), a magnetic state of the selected memory cell 20 ("0" or "1") may thus be determined.

The MTJ memory cells based on in-plane orientation of magnetization in free and
15 pinned magnetic layers suffer from several disadvantages:

- (a) MTJ element with in-plane orientation of magnetization in free and pinned magnetic layers require an elongated (rectangular, ellipse and the like) shape of the MTJ element with an aspect ratio (length/width) of 2 or higher in order to insure information storing and to reduce an error probability in the "write"
20 mode. This limits the density of MTJ cells in a MRAM array.
- (b) The specified elongated shape of the MTJ elements is difficult to reproduce in sub-micron range of dimensions across a MRAM array composed of thousand elements. The reduction of the MTJ element dimensions results in broadening of a statistical distribution of the element size and shape across the array.
25 Therefore, accidental reverse of the adjacent elements simply by the effect of the magnetic field produced along one of the addressing lines, bit or word, increases.
- (c) Number of addressing error in a MRAM array with in-plane orientation of magnetization increases with cell density increase.
- 30 (d) The MTJ elements with sub-micron dimensions suffer from instability at elevated temperature of operation.

All above-mentioned disadvantages limit an application of the MTJ memory cells with in-plane orientation of magnetization in the magnetic layers for high-density MRAM arrays.

A present invention addresses these needs. The invention provides a memory cell for a MRAM array with a perpendicular orientation of magnetization in the pinned and free layers of the MTJ element relative to a major plane of the tunnel barrier layer. The switching field of the MTJ element with the perpendicular magnetization does not require specific shape of the junction and marginally depends on a junction size. Hence, the switching field of the MTJ elements across the MRAM array has a high uniformity. The demagnetizing field in magnetic layers with the perpendicular anisotropy decreases with the reduction of the junction size resulting in an increase of the MTJ element stability. A use of a conductive magnetic flux guide reduces a write current and prevents unwanted magnetization reversal in the MTJ elements along the energized addressing lines.

BRIEF SUMMARY OF THE INVENTION

The memory cell according to the present invention includes a MTJ element and a magnetic flux guide electrically connected in series with a selection device, such as a transistor or similar non-linear element, and conductive lines. The MTJ element consists of a pinned magnetic layer and free magnetic layer with easy axis of magnetization oriented perpendicular to a major plane of the layers. A tunnel barrier layer is interposed between the pinned and free layers. The pinned layer has coercivity superior than that of the free layer.

The magnetic flux guide consists at least of a bottom magnetic portion and a top magnetic portion with the MTJ element positioned between the portions. The magnetic flux guide provides an effective magnetic flux supply to the MTJ element for reducing a write current in a "write" mode or an excitation current in a "read" mode of operation. The magnetic flux guide is made of a conductive magnetic material having a high magnetic permeability and a low electrical resistivity. The pinned and free layers of the MTJ element are magnetically isolated from the magnetic flux guide by thin non-

magnetic conductive spacers. This prevents undesirable effects of the magnetic flux guide on a magnetic state of the pinned and free layers.

Each memory cell employs a pair of conductive read lines and pair of conductive write lines. The pair of the conductive read lines includes a bit line and word line, which are orthogonal to one another, spaced from each other in a vertical direction and form an intersection region. The pair of the conductive write lines includes a write line and excitation lines, which are orthogonal to one another, electrically isolated from one another, positioned in a vertical space between the intersecting pair of the conductive read lines and define a corner at their intersection. The MTJ memory element along with the magnetic flux guide is arranged at the intersection region of the pair of the conductive read lines in a vertical space between the read lines and in the corner defined by the intersecting pair of the conductive write lines. The magnetic flux guide can further include a magnetic cap. The magnetic cap and the bottom magnetic portion can overhang fractions of the conductive write lines at their intersection region to enhance efficiency of the magnetic flux guide. One of the conductive read lines; for instance, the bit line can contact the MTJ element through the magnetic flux guide. The other conductive read lines; for instance, the word line is connected to the non-linear element. The write and excitation lines are position in the vicinity of the MTJ memory element and the magnetic flux guide, and are electrically isolated from them. The pairs of the conductive read and conductive write lines are co-parallel to one another, for instance, the bit line can be parallel to the write line and the word line can be parallel to the excitation line and vice-versa. All the lines are electrically isolated from one another.

The MTJ memory cell according to the present invention can have several embodiments, which are not limited to the following:

- to enhance spin-dependent tunneling, the MTJ element can employ at least one spin polarizing layer, which can be positioned on one or both sides of the tunnel barrier layer between the tunnel barrier layer and one or both magnetic layers;
- to stabilize domain structure of the pinned layer for reducing addressing errors, the MTJ element can employ an antiferromagnetic layer having direct contact with the pinned layer and providing an antiferromagnetic exchange coupling with the pinned layer;

- to increase memory cell density in the MRAM array, at least one of the read conductive lines can have a multilayer structure being composed at least of one magnetic conductive layer and one non-magnetic conductive layer having the magnetic conductive layer being positioned adjacent the MTJ element or the magnetic flux guide.

5 Switching field of TMJ memory element with perpendicular orientation of magnetization in the free and pinned layers has a marginal dependence on a junction size. This results from a weak dependence of the demagnetizing field in the pinned and free layers with a perpendicular anisotropy on the junction size. Therefore, the MRAM arrays with MTJ cells according to the present invention can have high density; high magnetic
10 stability, low error rate and high reliability. Positioning of the MTJ memory element between portions of the magnetic flux guide allows substantial reduction of the write current.

The following illustrate the objects and advantages of the present invention. The objects and advantages are provided here by way of examples, and not by way of
15 limitation.

Further objects, features and advantages of the present invention will become apparent from the following description of the preferred embodiments with reference to the attached drawings in which reference numbers indicate similar elements. In the drawings closely related figures have the same number but different alphabetic suffixes.

20 BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A and 1B illustrates a schematic sectional view of a conventional MTJ memory cell of a MRAM array with in-plane orientation of magnetization in pinned and
25 free layers in a “write” and “read” mode of operation, respectively.

Fig.2A and 2B illustrate a MH-loop and an RH-curve of MTJ element with perpendicular anisotropy in the free and pinned layers according to the present invention.

Fig.3 is a sectional side view of a first preferred embodiment of a MTJ memory cell according to the present invention in the “write” mode of operation.

30 Fig.4 is a top-down view of the first preferred embodiment of the MTJ memory cell according to the present invention shown in Fig.3.

(SiO₂) (not shown). The magnetic flux guide 37 includes a bottom magnetic portion 36 and a top magnetic portion 38 with the MTJ memory element 32 positioned between them.

The memory element 32 includes a pinned magnetic layer 54, a free magnetic layer 56, and a tunnel barrier layer 58 of alumina (Al₂O₃) interposed between the pinned 54 and free 56 layers. The MTJ memory element 32 is magnetically separated from the portions 36 and 38 of the magnetic flux guide 37 by non-magnetic conductive spacers 62 and 64 made of 10 nm thick platinum (Pt) film, which are placed on the both sides of the MTJ memory element 32. This restrains undesirable effects of the magnetic flux guide 37 on a magnetic state of the pinned 54 and free 56 layers. Moreover, the non-magnetic spacer 62 made of Pt provides an effective control of magnetic and crystalline properties of the pinned layer 54.

The magnetic pinned layer 54 and magnetic free layer 56 have an easy axis of magnetization oriented perpendicular to a major plane of the layers. The layers 54 and 56 are made of (Co_{0.5}/Pt_{1.5})_n multilayers, where *n* is a number of Co_{0.5}/Pt_{1.5} repeats. The number of the repeats can be *n* = 6 in the pinned layer 54 and *n* = 4 in the free layer 56. Layers of Co in the repeats of the pinned 54 and free 56 layers are positioned adjacent the tunnel barrier layer 58. The magnetization in the pinned 54 and free 56 layers has two stable states either “up” or “down”. The coercivity of the free magnetic layer 56 is about 200 Oe that is less than the coercivity of the pinned magnetic layer 54, which is about 600 Oe. As a result, the pinned layer 54 requires a stronger external magnetic field to change the magnetization orientation from “up” to “down” state or vice-versa than that to reverse the magnetization orientation in the free layer 56. So, the orientation of magnetization in the free layer 56 can be changed by a relatively small external magnetic field without affecting the magnetic state of the pinned layer 54. The orientation of the arrows shown in Fig. 3 (both “up”) represents a parallel configuration of the magnetization in the magnetic layers 54 and 56. This orientation corresponds to a low state of the resistance of the MTJ memory element 32 (logic “0”). The pinned layer 54 is placed under the free layer 56. However, the order of the pinned 54 and free 56 magnetic layers in the stack of the MTJ memory element 32 can be any.

Fig.5 is a top-down view of a portion of a MRAM array composed of the memory cells according to the first preferred embodiment of the present invention given in Fig.3 and Fig.4.

Fig.6 is a sectional side view of the first preferred embodiment of the MTJ cell according to the present invention in the “read” mode of operation.

Fig.7 is a sectional side view of a second preferred embodiment of a MTJ memory cell according to the present invention.

Fig.8 is a sectional side view of a third preferred embodiment of a MTJ memory cell according to the present invention.

Fig.9 is a sectional side view of a fourth preferred embodiment of a MTJ memory cell according to the present invention.

Fig.10 is a sectional side view of a fifth preferred embodiment of a MTJ memory cell according to the present invention.

Fig.11 is a top-down view of the fifth preferred embodiment of the MTJ memory cell according to the present invention shown in Fig. 10.

Fig.12 is a top-down view of a portion of a MRAM array composed of the memory cells according to the fifth preferred embodiment of the present invention given in Fig.10 and Fig.11.

Fig.13 is a sectional view of a six preferred embodiment of a MTJ memory cell according to the present invention.

Fig. 14 is a top-down view of the six preferred embodiment of the MTJ memory cell according to the present invention shown in Fig. 13.

Fig.15 is a top-down view of a portion of a MRAM array composed of the memory cells according to the six preferred embodiment of the present invention given in Fig.13 and Fig.14.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A MTJ memory cell of the present invention utilizes a phenomenon of a tunneling giant magnetoresistance in sandwiched magnetic and insulating layers. The memory cell employs a MTJ memory element formed by two magnetic layers with perpendicular

anisotropy having different coercive forces, which are separated by a thin insulating layer as a tunneling barrier.

Figs. 2A and 2B illustrate a MH-loop and a MR-curve of the MTJ element with the perpendicular anisotropy in the free and pinned magnetic layers when an external magnetic is applied perpendicular to a major plane of the layers. H_{CF} and H_{CP} is a coercivity of the free and pinned layers, respectively. Arrows denote orientation of the magnetization in the pinned and free layers. The dot arrow corresponds to the magnetization orientation in the free layer. The dash arrow represents the orientation of the magnetization in the pinned layer. A dot line in the Fig.2A represents a MH-loop of the free layer. A dash line gives the MH-loop of the pinned layer. The solid line represents a combined MH-loop of the MTJ element composed of the pinned and free layers having different coercivity. The Fig.2B shows an equivalent RH-loop of the MTJ element composed of the free and pinned layers.

According to the Figs.2A and 2B, the MTJ element has four stable magnetic states. Two of them with a parallel orientation of the magnetization in the pinned and free layers correspond to a low resistance state (or logic "0"). The other two states with the anti-parallel orientation of the magnetization in the free and pinned layers correspond to the high resistance state (or logic "1"). The mutual orientation of the magnetization in the layers can be changed by an external magnetic field applied perpendicular to the major plane of the layers. The coercivity of the free layer H_{CF} is lower than that of the pinned layer H_{CP} . Hence, the orientation of the magnetization in the free layer will change first when the external magnetic field is applied. The relative variation of the resistance between these two states may be up to 40% by appropriate selection of materials and their thickness.

A first preferred embodiment of the MTJ memory cell according to the present invention is illustrated in Fig.3 (a sectional side view) and Fig.4 (a top-down view). A memory cell 30 is formed on a substrate 31. The memory cell 30 comprises a MTJ memory element 32, a conductive magnetic flux guide 37, a transistor 34, a pair of conductive read lines 44 and 46, and a pair of conductive write lines 48 and 52. The conductive read lines 44 and 46, and the conductive write lines 48 and 52 are preferably are made of copper (Cu) and electrically isolated from each other by silicon dioxide

Fig.4 shows a top-down view of the memory cell 30. The conductive lines 44 and 52, and 46 and 48 are co-parallel. The pair of the conductive read lines includes a word line 44 and a bit line 46, which are preferably orthogonal to one another, intersect one another at an intersection region and spaced from one another in a vertical direction. The pair of the conductive write lines includes a write line 48 and an excitation line 52, which are also preferably orthogonal to one another, electrically isolated from one another and positioned in the vertical space between the intersecting pair of the conductive read lines 44 and 46. The bit line 46 is connected in series with the MTJ memory element 32, the conductive magnetic flux guide 37 and the transistor 34. The read line 44 is coupled to a gate of the transistor 34. The magnetic flux guide 37 and the memory element 32 are arranged at the intersection region of the pair of the conductive read lines 44 and 46 in the vertical space between the lines. In addition, the memory element 32 is positioned in the vicinity of a corner defined by the intersecting pair of the conductive write lines 48 and 52. The word 44 and bit 46 lines, as well the write 48 and excitation 52 lines may replace one another, for example, the bit line 46 can serve as the word line 44 and the word line 44 can serve as the bit line 46.

Fig.5 provides a top-down view of a portion of a MRAM array 300 composed of the memory cells 30 shown in Figs.3 and 4. The word lines 44a-d extend along columns of the MTJ memory elements 32a-e (marked as crosses). The bit lines 46a-b extend along rows of the MTJ memory elements. Besides the word and bit lines, the memory array 300 comprises the excitation lines 52a-d and the write lines 48a-b. The excitation lines 52a-d are arranged in parallel to the word lines 44a-d. The write lines 48a-b are arranged in parallel to the bit lines 46a-b. The bit 46a-b and word 44a-d lines are intersect each other at a plurality of the intersection regions and are spaced from each other in a vertical direction. The excitation 52a-d and write 48a-b lines also intersect each other, electrically isolated from each other and are positioned in the vertical space between the intersecting bit and word lines. The intersecting excitation and write lines define plurality of corners. The MTJ memory elements 32a-e are positioned at the intersections regions of the word and bit lines, and in the corners defined by the intersecting excitation and write lines. The plurality of the word lines 44a-d is connected to a first read circuitry 72. The plurality of the bit lines 46a-b is coupled to a second read circuitry 74. The write lines 48a-b and the

excitation lines 52a-d are connected to a first write circuitry 76 and a second write circuitry 78, respectively. The read circuitries 72 and 74 and the write circuitries 76 and 78 control an operation of the MRAM array 300 in the “read” and “write” modes applying signals of a predetermined polarity and magnitude.

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FABRICATION PROCESS FOR THE MEMORY CELL

Preferred materials, thickness, and process steps of the MTJ cell 30 are described with the reference to the Figs.3-5. The MRAM array 300 is formed on a planar surface of a silicon wafer 31 covered by an insulating layer of SiO_2 (not shown). The wafer 31 includes the earlier formed transistor 34. The word line 44 made of Cu and the bottom magnetic portion 36 made of $\text{Ni}_{79}\text{Fe}_{21}$ -alloy are formed on the substrate 31 one after another. They are electrically isolated from one another and covered with a insulating layer of SiO_2 (not shown). Then, a top surface of the insulating SiO_2 layer is planarized by a chemical-mechanical polish (CMP) to expose a top surface of the bottom portion 36 of the magnetic flux guide 37. The MTJ memory element 32 is formed on the common planar surface composed by the SiO_2 -layer and the bottom magnetic portion 36. Next, series of layers, which include the non-magnetic spacer 62, the MTJ memory element 32, the non-magnetic spacer 64 and a layer of $\text{Ni}_{79}\text{Fe}_{21}$, are deposited by a vacuum sputter deposition. The layer of $\text{Ni}_{79}\text{Fe}_{21}$ represents a bottom part of the top magnetic portion 38.

In order, the 10 nm thick platinum (Pt) spacer 62, the $(\text{Co}_{0.5}/\text{Pt}_{1.5})_6/\text{Co}_{0.5}$ pinned layer 54 are deposited. On a top of the pinned layer 54, 1 nm of Al is deposited and oxidized in a vacuum chamber with an oxygen enriched atmosphere and elevated temperature to form the insulating tunneling barrier layer 58 of Al_2O_3 . Then, the free magnetic layer 56, the non-magnetic conductive spacer 64, and the bottom part of the top magnetic portion 38 are deposited. The free layer 56 is formed of the $(\text{Co}_{0.5}/\text{Pt}_{1.5})_4$ multilayers with the Co-layer facing the tunnel barrier layer 58 of Al_2O_3 . A 0.1- μm thick layer of $\text{Ni}_{81}\text{Fe}_{19}$ covers the spacer 64 made of 10 nm thick Pt layer. At this point, there is a single large MTJ memory element that covers the entire surface of the substrate. This large MTJ element is then patterned into many small MTJ memory elements similar to the element 32 by photoresist masking and ion milling down through the stack of the

layers to the CMP planarized top surface of the bottom magnetic portion 36 and the insulating layer of SiO₂. State-of-the-art silicon VLSI processes are then used to form write 48 and excitation 52 lines in an insulator of SiO₂ (not shown) and opened a contact hole in SiO₂ to the 0.1- μ m thick layer of Ni₈₁Fe₁₉ that covers the non-magnetic spacer 64.

5 Electroplating of Ni₈₁Fe₁₉ alloy into the contact hole forms the top magnetic portion 38 of the flux guide 37. Another CMP process is applied above the surface of SiO₂ to expose a top surface of the top magnetic portion 38. Then, the bit line 46 of Cu is formed on a common planar surface of SiO₂ and the top magnetic portion 38 using state-of-the-art silicon VLSI processes. The bit line 46 has direct electrical contact with the MTJ memory
10 element 32 through the electrically conductive top portion 38 of the magnetic flux guide 37.

OPERATION OF THE MEMORY CELL

15 MTJ memory elements of the present invention may have two “write” and two “read” modes of operation. The mode of operation depends on a strength of a magnetic fringing field produced by the magnetic pinned layer 54 relative to the coercivity of the free layer 56. The fringing field is produced by magnetic charges accumulated on a surface of the pinned layer 54 that is adjacent the free layer 56. If the fringing field of the
20 pinned layer 54 is less than the coercivity of the free layer 56, the information can be stored in the free layer 56 of the MTJ memory element 32. At this condition, the fringing field upon writing completion will not reverse the orientation of magnetization in the free layer 56. However, if the coercivity of the free layer 56 is less than the fringing field of the pinned layer 54, the orientation of magnetization in the free layer 56 can be forced by
25 the fringing field in parallel to the orientation of magnetization in the pinned layer 54 when the write current is removed. At this condition, the information can be written to the pinned layer 54 of the MTJ memory element 32.

The “write” mode of operation of the memory cell 30 is described with a reference to Figs.3 and 4. In the “write” mode the transistor 34 is blocked applying an
30 appropriate bias signal to its gate through the word line 44. Writing to the MTJ memory element 32 is accomplished by passing simultaneously write currents I_{W1} and I_{W2} through

the intersecting write line 48 and excitation line 52, respectively. The currents I_{W1} in the write line 48 and I_{W2} in the excitation line 52 generate magnetic fields 49 and 51, respectively. The magnetic fields 49 and 51 have the same polarity and are concentrated in the magnetic flux guide 37 that has a high magnetic permeability. The fields 49 and 51 are applied perpendicular to the major plane of the free 56 and pinned 54 layers.

When the coercivity of the free layer 56 is greater than the fringing field of the pinned layer 54, the information is written to the free layer 56. The magnetic field produced by either I_{W1} or I_{W2} alone in the MTJ memory element 32 is less than the magnetic field required to change the orientation of magnetization in the free layer 56.

Therefore, half-selected elements 32b-e schematically shown in Fig.5, those over which only I_{W1} or I_{W2} alone is passing, are not written. However, the combination of magnetic fields from the currents I_{W1} and I_{W2} is sufficient to write to the free layer 56 of the selected memory element 32a, which is positioned in a corner defined by the intersecting write 48a and excitation 52a lines. A strength of the combined magnetic field is selected to be superior the coercivity of the free layer 56 and less than the coercivity of the pinned magnetic layer 54. In principal, only the memory element 32a located at the intersection of the write line 48a and excitation line 52a is subject to magnetization reversal in the free layer. Separately magnetic fields produced by write line 48a and excitation line 52a are insufficient to cause reversal of magnetization in the free layer of the elements 32b-e. The magnetic flux guide promotes a strength of the write magnetic field affecting the memory element and allows a reduction of the write currents.

If the fringing field of the pinned layer 54 exceeds the coercivity of the free layer 56, the orientation of magnetization in the pinned 54 and free 56 layers coincide (both “up” or both “down”) when the write currents are removed. At this condition, the information can be written to the pinned layer 54 of the MTJ memory element 32. The strength of the combined magnetic field produced by two write currents I_{W1} and I_{W2} simultaneously should exceed the coercivity of the pinned layer 54. Therefore, separately strength of the fields 49 and 51 should be less than the pinned layer coercivity to restrain magnetization reversal in half-selected elements 32b-e.

Likewise the “write” modes, the MTJ memory elements according to the present invention can have two “read” modes of operation. The “read” mode of the memory cell

30 is described with reference to Fig. 6. In the “read” mode the transistor 34 is opened applying an appropriate signal to its gate through the word line 44. A sense current I_S in the transistor 34 is at a maximum. The sense current I_S flows through the bit line 46, the top magnetic portion 38, the MTJ element 32, the bottom magnetic portion 36, and the opened transistor 34. This current I_S enables the resistance of the MTJ element 32 to be measured. If the information was written to the free layer 56, the resistance of the MTJ element 32 depends on the magnetization orientation in the free layer 56 relative to the fixed magnetization orientation in the pinned layer 54. By comparison the resistance of the MTJ memory element 32 with a reference MTJ memory element (not shown), the state of the given memory cell (“1” or “0”) can be determined.

If the information was written to the pinned layer 54, the “read” mode requires use of the excitation current I_{EX} in the excitation line 52 (Fig.6). The excitation current I_{EX} produces the excitation magnetic field 53 of the predetermined polarity and strength. The strength of the excitation field is insufficient to reverse the orientation of magnetization in the pinned layer 54 to where the information was written. However, the excitation field 53 is strong enough to overcome the fringing field of the pinned layer 54 and to orient the magnetization in the free layer 56 in parallel to the excitation field 53. The magnetic state of the MTJ memory cell 30 (“0” or “1”) can be identified comparing resistance of the element 32 with that of the reference memory element (not shown).

In the described above the first preferred embodiment, the word line 44 can also be referred to as a first electrically conductive line, while the bit line 46 can also be referred to as a second electrically conductive line. As will be appreciated, both the first electrically conductive line 44 and the second electrically conductive line 46 can be positioned at any number of locations relative the MTJ memory element 32. The write line 48 can also be referred to as a third electrically conductive line, while the excitation line 52 can also be referred to as a fourth electrically conductive line. The write line 48 and the excitation line 52 are arranged between the intercepting word line 44 and bit line 46 adjacent the MTJ memory element 32. All the lines are electrically isolated from one another.

Figs 7-15 illustrate several preferred alternative embodiments of the present invention, which employ similar modes of operation and manufacturing processes.

Fig.7 shows a second preferred embodiment according to the present invention. In the memory cell 40 the bottom portion 36 of the magnetic flux guide 37 is made thicker than the top portion 38. As a result, the MTJ memory element 32 is positioned above the write 48 and excitation 52 lines. This design can have higher yield since the MTJ memory element 32 is formed at a final stage of a manufacturing process after formation of the write 48 and excitation 52 lines.

Fig.8 illustrates a third preferred embodiment according to the present invention. In the memory cell 50 the bit line 46 is made of multiplayer and comprises at least two electrically conductive layers 82 and 84. The layer 82 is made of magnetic material having a high permeability, for instance of $\text{Ni}_{81}\text{Fe}_{19}$, which is positioned adjacent the bottom magnetic portion 36. The bottom magnetic portion 36 and the magnetic layer 82 compose the magnetic flux guide 37. The MTJ memory element 32 is positioned inside the magnetic flux guide 37. The layer 84 can be made of Cu. The top surface of the bottom magnetic portion 36 is planarized by CMP. The MTJ memory element 32 is magnetically separated from the bottom magnetic portion 36 and the magnetic layer 82 by non-magnetic conductive spacers 62 and 64, respectively. The pinned layer 54 can be made of 10-nm thick single layer of TbFeCo-alloy having a perpendicular anisotropy. To promote a giant magnetoresistance in the TMJ memory element 32, 1-nm thick spin-polarizing layer 66 of CoFe having a high spin polarization is placed between the pinned magnetic layer 54 and the tunnel barrier layer 58. The spin-polarizing layer 66 can be made of multilayer, such as $\text{Pt}_1/\text{CoFe}_1$ or similar with the layer of CoFe being in contact with the tunnel barrier layer 58. The free layer 56 can be made of 5-nm thick single layer of GdFeCo-alloy with a spin-polarizing layer 68 sandwiched between the free layer 56 and the tunnel barrier layer 58. MRAM arrays based on the cell 50 have a high output signal in the “read” mode, simplified manufacturing process and potentially higher yield.

Fig.9 shows a fourth preferred embodiment according to the present invention. The MTJ element 32 of the memory cell 60 has reversed order of the pinned 54 and free 56 layers in the stack. The free layer 56 is deposited first on the top planar surface of the bottom magnetic portion 36. A formation of the free layer 56 on the planar surface allows an effective control of magnetic properties of the free layer 56, such as a coercivity and a dispersion of a magnetic anisotropy. A reduction of the free layer coercivity facilitates

switching of the free layer 56 in the “write” mode. The pinned magnetic layer 54 is placed above the free layer 56 and is separated from the free layer 56 by the tunnel barrier layer 58. The coercivity of the pinned layer 54 can be effectively controlled using an antiferromagnetic exchange coupling between the magnetic pinned layer 54 and the non-magnetic conductive spacer 64 made of an antiferromagnetic material, for instance, $\text{Fe}_{50}\text{Mn}_{50}$ alloy. A thickness of the antiferromagnetic $\text{Fe}_{50}\text{Mn}_{50}$ spacer can be of 10 nm. The exchange coupling between the magnetic pinned layer 54 and the antiferromagnetic spacer 64 improves a stability of domain structure in the pinned layer 54 and thus prevents undesirable reversal of the magnetization in the pinned layer. The MTJ memory element 32 of the memory cell 60 has a reduced write current due to a low coercivity of the free layer 56 and improved magnetic stability of the pinned layer 54.

Figs.10-12 show a fifth preferred embodiments of the present invention. The memory cell 70 employs three pieces structure of the magnetic flux guide 37, which includes the bottom portion 36, the top portion 38 and a magnetic cap 42. The pieces 36, 38 and 42 of the magnetic flux guide 37 are preferably made of soft magnetic material such as $\text{Ni}_{81}\text{Fe}_{19}$ -alloy having a high magnetic permeability and a low electrical resistivity.

The MTJ memory element 32 (not shown in Fig.11) is positioned at an intersection region of the conductive read lines 44 and 46, and in a corner defined by the intersecting pair of the conductive write lines 48 and 52. The lines 44 and 52, and 46 and 48 are co-parallel. The bottom magnetic portion 36 and the magnetic cap 42 overhang the top magnetic portion 38 and fractions of the write lines 48 and 52 at their intersection. This improves a magnetic coupling between the write lines 48 and 52, and the magnetic flux guide 37 allowing a reduction of the write or excitation currents in the “write” or “read” mode, respectively.

A part of a MRAM array 700 composed of the cells 70 is shown in Fig.12. The magnetic caps 42a-e of the adjacent memory cells are magnetically isolated from each other by non-magnetic gaps. For instance, the magnetic cap 42a is magnetically isolated from the adjacent magnetic caps 42b and 42e by the non-magnetic gaps 92a and 92b, respectively. Similarly, the bottom magnetic portions (not shown) of the adjacent memory cells are magnetically isolated from each other by the non-magnetic gaps.

Figs.13-15 show a six preferred embodiments of the present invention. The memory cell 80 has a three pieces structure of the magnetic flux guide 37, which includes the bottom portion 36, the top portion 38 and the magnetic layer 82 of the bit line 46.

The read lines 44 and 46 have a multilayer structure and comprise at least of two
5 conductive layers, one of them is made of magnetic material with a high permeability such as $\text{Ni}_{81}\text{Fe}_{19}$. To facilitate a manufacturing process of the memory cell 80, the bottom portion 36 of the magnetic flux guide 37 is made simultaneously with the word line 44 and also employs the multilayer structure. The magnetic layer 82 of the bit line 46 and the magnetic layer 88 of the bottom magnetic portion 36 are positioned adjacent the MTJ
10 memory element 32. Along with the top magnetic portion 38 they form the flux guide 37 to provide an effective supply of the signal magnetic field to the MTJ memory element 32. Layers 86 and 84 of the word line 44 and the bit line 46 can be made of Cu, having a low electrical resistivity. A thickness of the magnetic 82, 88 and conductive 84,86 layers can be about 0.2 μm and 0.5 μm , respectively. The word line 44 of the memory cell 80
15 can be positioned at various places relative to the bottom 36 and top 38 magnetic portions.

While the above description contains many specifics these should not be construed as limitations on the scope and spirit of the present invention, but rather as an exemplification of the preferred embodiments. Many other variations are possible. For
20 example, shape and dimensions of the bottom magnetic portion 36 and magnetic cap 42, a position of the conductive write lines 48 and 52, a position of the conductive read lines 44 and 46 relative to the MTJ memory element 32. As well, a number of layers in the conductive lines, in bottom and top magnetic portions of the magnetic flux guide, and in the magnetic cap can be any. The following materials can be used to form basic
25 components of the memory cells.

The free magnetic layer 56 can be made from a group of conductive magnetic materials exhibiting a perpendicular anisotropy. These materials include but are not limited to layers or laminates based on Co, Fe, Ni, Pt, Pd, Tb, Gd, B, Cr and their alloys. Specific examples of laminates and layers include, but are not limited to Co/Pt, CoFe/Pt,
30 CoFeB/Pt, CoFe/Pd, Fe/Pt, GdFe, GdFeCo or similar. The coercivity of the free ferromagnetic layer 56 can be in a range from 50 Oe to 1000 Oe and more specifically, in

a range from 100 Oe to 300 Oe. Thickness of the free layer can be from 0.2 nm to 100 nm and more specifically, from 5 nm to 20 nm.

5 The pinned ferromagnetic layer 54 can be made of conductive magnetic material having a perpendicular anisotropy. These materials include but are not limited to layers or laminates based on Co, Fe, Ni, Pt, Pd, Tb, Gd, B, Cr and their alloys. Specific examples of laminates and layers include, but are not limited to TbFe, TbFeCo, Co/Pt, Co/Pd, CoFe/Pt, CoFeB/Pt, CoFe/Pd, CoFeB/Pd, CoCrPt/CoFe, FePt or similar. The coercivity of the pinned magnetic layer 54 should be higher than that of the free magnetic layer 56. As a result, the coercivity of the pinned magnetic layer 54 can be in a range from 100 Oe to 5000 Oe and more specifically from 200 Oe to 600 Oe. Thickness of the pinned layer 10 can be in a range from 0.5 nm to 200 nm, and more specifically, from 10 nm to 40 nm.

The tunnel barrier layer 58 can be made of insulating or partially conductive materials. Examples of suitable materials for the tunnel barrier layer 58 include but are not limited to semiconductor films, such as Si, Ge, oxides of metallic and semiconductor 15 films, such as Al₂O₃, TiO₂, Ta₂O₅, SiO₂, and their based alloys or metallic particles incorporated into the insulating films. The barrier layer can have single layer or multilayer structure composed of laminates of insulating and metallic films. Thickness of the tunnel barrier layer 58 can be in a range from 0.2 nm to 5 nm, and more specifically, from 1 nm to 2 nm.

20 In the present embodiments the bottom 36 and top 38 magnetic portions, the magnetic cap 42 and the magnetic conductive layer 82 and 88 are made of soft magnetic material having a low electrical resistivity and high magnetic permeability. Examples of materials for these magnetic elements and layers include but are not limited to alloys and laminates of Co, Fe, Ni, B, Zr, Hf, Cr, Ru, Cu, such as NiFe, CoNiFe, CoFe or similar. 25 The bottom 36 and top 38 magnetic portions can have a thickness of approximately from 50 nm to 5000 nm, and, more specifically, in a range from 100 nm to 1500 nm. Thickness of the magnetic cap 42 and magnetic layers 82 and 88 can be in a range from 50 nm to 1000 nm and, more specifically, in a range from 100 nm to 250 nm.

Materials for the spin-polarizing layers 66 and 68 include but are not limited to 30 Co, Fe or their based alloys such as CoFe, CoFeB or similar. Thickness of the spin-

polarizing layers can be in a range from 0.2 nm to 20 nm and, more specifically, from 0.4 nm to 2 nm.

The electrically conductive lines 44, 46, 48 and 52 and their conductive layers 84 and 86 discussed herein can be made of Al, Cu, Pt, Au, Ta, W, their based alloys or
5 laminates.

The antiferromagnetic spacer 64 in the cell 60 can be made of conductive Mn-based alloys, such as FeMn, IrMn, PtMn or similar.

Embodiments of the present invention may include different forms. The description herein provides an exemplification of the principles of the invention and is
10 not intended to limit the invention to the particular embodiments illustrated.

The structural embodiments of the present invention illustrated herein are believed to reduce accidental reversals of the magnetization in MTJ memory elements adjacent one of the write lines 48 or along one of the excitation lines 52 energized in “write” and “read” modes of operation.

15 Although the specific embodiments have been illustrated and described herein, those of ordinary skill in the art will appreciate that an arrangement calculated to achieve the same techniques could be substituted for the specific embodiments shown. This disclosure is intended to cover adaptations or variations of the embodiments of the invention. It is to be understood that the above description has been made in an
20 illustrative fashion, and not a restrictive one.

Combination of the above embodiments, and other embodiments not specifically described herein will be apparent to those of skill in the art upon reviewing the above description. The scope of the various embodiments of the invention includes other applications in which the above structures and methods are used. Therefore, the scope of
25 various embodiments of the invention should be determined with reference to the appended claims, along with the full range of equivalents to which such claims are entitled.

Accordingly, the scope of the invention should be determined not by the embodiments illustrated, but by appended claims and their legal equivalents.